**What is claimed is:**

1     1.     A method of processing a plurality of Z vectors, each Z vector including Z elements,

2     each element including K bits, where Z is a positive integer greater than 1 and K is a positive

3     integer greater than zero, the plurality of Z vectors corresponding to a binary codeword, portions

4     of said binary codeword having a direct mapping relationship to a plurality of transmission units,

5     said plurality of Z vectors being stored in a set of D memory arrays, where D is an integer

6     greater than zero, each memory array including Z rows of memory locations, each memory

7     location of a row corresponding to a different array column, each array column corresponding to

8     a different one of said plurality of Z vectors, each Z vector identifying one column in each of

9     said D memory arrays, the method comprising:

10          generating a series of sets of control information, each set of control information

11    including:

12                    i) a transmission unit identifier;

13                    ii) a Z vector identifier;

14                    iii) a row identifier; and

15          for at least one generated set of control information:

16                    reading P times K divided by D bits, where P is a positive integer greater than

17    zero, from each column identified by the Z vector identified by the Z vector identifier included

18    in said at least one generated set of control information.


1     2.     The method of claim 1,

2          wherein said method of processing is performed by a transmission device prior to

3     transmission of said transmission units;

4                    wherein D is 1; and

5                    wherein K is 1.


1     3.     The method of claim 2, further comprising:

2          for said at least one generated set of control information:

3                    generating from said P bits read from memory, a portion of the transmission unit

4          identified by the transmission unit identifier included in said at least one generated set of

5          control information.

1     4.     The method of claim 3,

2     wherein said plurality of Z vectors includes n of said plurality of Z vectors, where n is a

3     positive integer greater than 1; and

4     wherein generating a series of sets of control information further includes:

5     incrementing a Z vector identifier value by n divided by M, where M is the

6     number of portions of the transmission unit having a direct mapping relationship to a

7     portion of the binary codeword said portion of the binary codeword including M times P

8     bits.

1     5.     The method of claim 4,

2     wherein each portion of a transmission unit is a symbol; and

3     wherein the transmission unit is a dwell.

1     6.     The method of claim 3, wherein generating a series of sets of control information further

2     includes:

3     incrementing the Z vector identifier value M times;

4     after incrementing the Z vector value M times:

5     i) resetting the Z vector identifier value to the Z vector identifier value existing at

6     the start of said incrementing; and

7     ii) incrementing a row identifier value by P.

1     7.     The method of claim 6, wherein generating a series of sets of control information further

2     includes:

3     after incrementing the row identifier value Z divided by P times, where Z divided by P

4     times is an integer,

5     setting the row identifier value to zero; and

6     incrementing the Z vector identifier value by a preselected positive integer value.

1     8.     The method of claim 7, wherein said preselected positive integer value is one.

1     9.     The method of claim 2, wherein said binary codeword is a low density parity check

2     codeword.

1　10.　The method of claim 1,

2　　　wherein said method of processing is used to process received transmission units; and

3　　　wherein K is an integer greater than zero and is a number of bits used to represent a soft

4　value corresponding to one bit of said binary codeword.


1　11.　The method of claim 10, where D is equal to K or 1.


1　12.　The method of claim 11, further comprising:

2　　　for said at least one generated set of control information:

3　　　　supplying the P bits read from memory to a demodulator.


1　13.　The method of claim 10, further comprising:

2　　　for said at least one generated set of control information:

3　　　　generating from said P bits read from memory, a portion of the transmission unit

4　　　identified by the transmission unit identifier included in said each generated set of

5　　　control information.


1　14.　The method of claim 13,

2　　　wherein said plurality of Z vectors includes n of said Z vectors, where n is a positive

3　integer greater than 1; and

4　　　wherein generating a series of sets of control information further includes:

5　　　　incrementing a Z vector identifier value n divided by M, where M is the number

6　　　of portions of the transmission unit having a mapping relationship to a portion of the

7　　　binary codeword said portion of the binary codeword including M times P bits.


1　15.　The method of claim 13, wherein generating a series of sets of control information

2　further includes:

3　　　incrementing a row identifier value by P　　incrementing the Z vector identifier value

4　M times;

5　　　after incrementing the Z vector value M times:

6　　　　i) resetting the Z vector identifier value to the Z vector identifier value existing at

7　　　　the start of said incrementing; and

8　ii) incrementing a row identifier value by P.

1    16.    The method of claim 15, wherein generating a series of sets of control information

2    further includes:

3        after incrementing the row identifier value Z divided by P times, where Z divided by P

4    times is an integer,

5        setting the row identifier value to zero; and

6        incrementing the Z vector identifier value by a preselected positive integer value.


1    17.    The method of claim 16, wherein said preselected positive integer value is one.


1    18.    The method of claim 10, wherein said binary codeword is a low density parity check

2    codeword.


1    19.    An apparatus for processing a plurality of Z vectors, each Z vector including Z elements,

2    each element including K bits, where Z is a positive integer greater than 1 and K is a positive

3    integer greater than zero, the plurality of Z vectors corresponding to a binary codeword, portions

4    of said binary codeword having a direct mapping relationship to a plurality of transmission units,

5    said apparatus comprising:

6        memory including a set of D memory arrays for storing said plurality of Z vectors, where

7    D is an integer greater than zero, each memory array including Z rows of memory locations,

8    each memory location of a row corresponding to a different array column, each array column

9    corresponding to a different one of said plurality of Z vectors, each Z vector identifying one

10    column in each of said D memory arrays;

11        memory access control module for generating a series of sets of control information,

12    each set of control information including:

13        i) a transmission unit identifier;

14        ii) a Z vector identifier;

15        iii) a row identifier; and

16        means for reading P times K divided by D bits, from said memory, where P is a positive

17    integer greater than zero, from each column identified by the Z vector identified by the Z vector

18    identifier included at least one generated set of control information.

1    20.    The method of claim 1,

2          wherein D is 1; and

3          wherein K is 1.


1    21.    The method of claim 19, wherein said memory access control modules includes:

2          a first counter for generating said Z vector identifier; and

3          a second counter for generating said row identifier.


1    22.    A machine readable medium comprising machine executable instructions for controlling

2    a computer device to process a plurality of Z vectors, each Z vector including Z elements, each

3    element including K bits, where Z is a positive integer greater than 1 and K is a positive integer

4    greater than zero, the plurality of Z vectors corresponding to a binary codeword, portions of said

5    binary codeword having a direct mapping relationship to a plurality of transmission units, said

6    machine executable instructions including instructions used to control the computer device to:

7          generate a series of sets of control information, each set of control information including:

8                i) a transmission unit identifier;

9                ii) a Z vector identifier; and

10                iii) a row identifier; and

11          for at least one generated set of control information:

12                read P times K divided by D bits, where P is a positive integer greater than zero,

13          from each column identified by the Z vector identified by the Z vector identifier included

14          in said at least one generated set of control information.